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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,311	01/26/2004	Dennis Wendell	SUNMP383	9410

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,311	WENDELL ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-23 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-11,14-17,19-23,27 and 29* is/are rejected.

7)☒ Claim(s) *8,13,18,25,26 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 06-06-05 has been received and entered in the case. New grounds of rejection necessitated by the amendment are set forth below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 14, the recitation "a pair of charging devices each being configured to supply a steady voltage to a separate one of the pair of input nodes upon receipt of a recovery activation signal" is indefinite because it is not clear. The gates of "a pair of charging devices" receive "a recovery activation signal". In claim 15, the same "pair of charging devices" having gates connected to ground.

Claim 15 is indefinite because of the technical deficiencies of claim 14.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6, 7, 9-11, 16 and 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Su et al. (USP. 6,275,435).

Regarding claims 1-4 and 6, figure 1 of Su shows a sense amplifier comprising an input stage having a pair of balanced isolation devices: PMOS (13_1) and PMOS (13_2) having gates connected to a common bias voltage (DATA_EN) generate by a bias generator circuit (not shown), a sense stage having a pair of sense nodes ($N11B_2$, $N11_2$) receiving output signals from the pair of balanced isolation devices (13_1) and (13_2), a pair of booster circuits (18_1, 18_2) to assist in a high -to-low state transition of a separate one of the pair of sense nodes during sense operation. Note that when a low voltage is applied to the gates of transistors (18_1, 18_2), a high voltage (Vdd) is applied to the pair of sense nodes ($N11B_2$, $N11_2$). The sense nodes ($N11B_2$, $N11_2$) are connected to the output of pair of balanced isolation devices PMOS (13_1) and PMOS (13_2).

Regarding claim 7, the transmission gate (12) receives an equalization control signal (EQUALIZE).

Regarding claims 9-11 and 16, figure 1 of Su shows a sense amplifier comprising a pair of input nodes receiving signals (DLB, DL), a pair of balanced isolation devices: PMOS (13_1) and PMOS (13_2) having gates connected to a common bias voltage (DATA_EN) generated by a bias generator circuit (not shown), a pair of sense nodes ($N11B_2$, $N11_2$) receiving output signals from the pair of balanced isolation devices (13_1) and (13_2), a transmission gate (12) receives an equalization control signal (EQUALIZE), a "pull down logic" (11_1, 19_1) and a pair of booster circuits (18_1, 18_2) to assist in a high –to-low state transition of a separate one of the pair of sense nodes during sense operation. The transmission gate (12), comprising PMOS device, receives an equalization control signal (EQUALIZE).

Regarding claim 19, figure 6 shows the detail of the sense amplifier (SA) of figure 1 comprising a "pull down logic" (MN0, MN1). The connections between the NMOS devices and the pair of sense nodes are clearly shown.

Regarding claims 20-23, figures 1 and 6 of Su shows a method for making a sense amplifier, comprising:

connecting a pair of input nodes to each receive a separate one of a pair of differential input signals (DL, DLB);

connecting an input of each of a pair of balanced isolation devices (PMOS 13_1) and (PMOS 13_2) to a separate one of the pair of input nodes, wherein each of the pair of balanced isolation devices has an output representing a separate one of a pair of sense nodes;

connecting a gate of each of the pair of balanced isolation devices to receive a common bias voltage (DATA_EN)

connecting each of a first terminal and a second terminal of a transmission gate (PMOS 12) to a separate one of the pair of sense nodes, the transmission gate (12) receives an equalization control signal (EQUALIZE);

connecting "pull down circuitry" (SA) to the pair of sense nodes: and

connecting each of a pair of booster devices (18_1, 18_2) to a separate one of the pair of sense nodes, each of the pair of booster devices being configured to assist a low-to-high state transition of the sense node to which the booster device is connected during a sensing operation. Note that when a low voltage is applied to the gates of transistors (18_1, 18_2), a high voltage (Vdd) is applied to the pair of sense nodes ($N11B_2$, $N11_2$).

Regarding claim 29, figure 1 and 6of Su shows a "pull down circuitry" comprising a pair of NMOS transistors (MNO, MN1). The connections between the NMOS devices and the pair of sense nodes are clearly shown.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure (US Pat. 5,455,802).

Regarding claims 5, 17 and 17, figure 2 of McClure includes all the limitations of these claims except for the limitation that the common bias voltage is

maintained at a level about one-half of a supply voltage level. However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the common bias voltage at a level about one-half of a supply voltage level dependent upon particular environment of use to ensure optimum performance. Note that the PMOS transistors (T3) and (T4) need a voltage slightly higher than the threshold of the PMOS transistors to turn them off.

Allowable Subject Matter

Claims 14 and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 8, 13, 18, 25, 26 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 14 and 15 would be allowable because the prior art of records (USP. 6,275,435) fails to teach or suggest a sense amplifier comprising a pair of charging devices as called for in claim 14.

Claims 8, 13, 18, 25, 26 and 28 are objected to because the prior art of records fails to teach or suggest a pair of booster devices comprising NAND gates as called for in claims 8, 13 and 25; a pair of charging devices or a recovery stage comprising PMOS transistors for charging the pair of input nodes as called for in claims 18, 26 and 28.

Response to Arguments

In the Remarks, page 10, the Applicant argues that circuit 221 is not a latch and shows that the latch must be the circuit of figure OA1 in page 12. However, there are many different types of latch. One of them that is well known in the art is a cross-coupled pair of transistors (see, figure 3 of USP. 6,263,460 or figure 6 of USP. 6,756,841). Thus, the objection of the specification is proper. Though the Applicant is entitled to be their own lexicographer, the lexicographer does not make the application distinguish over the prior art by giving the circuit different label.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

08-04-05

TUAN T. LAM
PRIMARY EXAMINER